Remarks

I. Status of the Claims

In the Office Action, the Examiner indicated that claims 1-16 are pending, and are rejected.

II. Rejections based on Prior Art – 35 USC §102

On page 2 of the Office Action, the Examiner states: "Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Olsen (US 5,440,538)" hereinafter "Olsen".

Olsen teaches of a system for transmitting data over an electronic signaling bus having a number of "communication links" 12a-12h, and one or more redundant (spare) links (19a in Fig. 2). In Olsen, if there are no faults in the non-spare links, the spare link is not used, and therefore does not teach using all functionally good links to transmit data. See Olsen, Fig. 2, where signal 19a is not used when non-spare links 12a-12h are all functional. Olsen extends his capability to transmit all eight bits per beat to multiple failures in the non-spare links by using additional spare links (see Figs. 7A, 7B). If Olsen has more failures than spare links, Olsen's bus must report a failure, and is unable to transfer data.

In stark contrast, Applicants' invention is directed to a system for transmitting data, the system having no redundant (spare) links. Applicants' invention instead, determines how many links are functional, and, using embodiments taught in Applicants specification, uses additional bus cycles (beats) to transfer a block of data. Applicant's invention requires NO spare links, which add to a cost of Olsen's system.

Applicants respectfully submit that, referring to Applicant's Claim 13, that Olsen does not teach "...utilizing all of the nonfaulty signaling conductors in the signaling bus", since Olsen's redundant links are only used if a fault occurs in a non-spare link. Similarly, Olsen's handling of multiple failures in Olsen's non-redundant links becomes even more wasteful, as additional spare links are required (Olsen's Fig. 7A, 7B), but are only used to transmit data to the extent that non-spare links are faulty.

Applicants therefore, respectfully ask that the Examiner reconsider and withdraw his rejection of Claim 13 under 35 U.S.C. 102(b).

Applicants believe that Claim 13 is allowable, and that therefore, dependent Claims 14, 15, and 16 are also allowable and ask that the Examiner withdraw his rejections of Claims 14, 15, and 16.

III. Rejections based on Prior Art – 35 USC §103

On page 3 of the Office Action, the Examiner states: "Claims 1-2, 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olsen (US 5,440,538) and in further view of Izuno et al. (US 5,717,852)." Hereinafter "Olsen" and "Izuno".

As described above, Olsen teaches of use of redundant links (signaling conductors), wherein Applicants teach of transmitting a block of data using all nonfaulty signaling conductors.

Izuno teaches of a multiple bus system. When a failure occurs during transmission, on a first bus, of a block of data, using Izuno, the block of data is kept and subsequently transmitted on a second, non-faulty bus. Izuno, like Olsen, has no teaching, suggestion, or motivation to transmit data on every nonfaulty signaling conductor. Olsen uses redundant links; Izuno uses completely separate busses.

Applicants respectfully direct the Examiner to Applicant's Claim 1, in particular to the claim element, "***transmitting the "J" bit block of data over the "K-F" nonfaulty signaling conductors using "J/(K-F)" beats, plus an additional beat if a remainder exists***." Olsen uses the same number of beats in every transmission, using spare links in order that the exact same number of bits is transmitted on every beat. Therefore, Olsen carries no notion of this claim element. Similarly, Izuno always transmits his block of data using the exact same number of beats, using a nonfaulty bus. If a failure occurs in Izuno during transmission, some beats are "lost", but in fact, the entire block of data is always transmitted using a fixed number of beats.

Since neither Olsen nor Izuno individually or in combination, teach, suggest, or motivate all the elements of Claim 1, Applicants respectfully request that the Examiner reconsider and withdraw his rejection of Claim 1 and its dependent claims (directly or indirectly, Claims 2-7).

Claim 2 depends from Claim 1. Applicants believe that Claim 1 is allowable, and therefore Claim 2 is allowable. However, Applicants now directly address the Examiner's rejection of Claim 2 under Olsen and Izuno. In Izuno, the entire block of data is retained in Izuno's sending unit (e.g., Izuno's bus-master or bus-slave). As noted above, the entire block of data, upon detection of a fault, is subsequently re-transmitted on a completely separate bus. Applicants respectfully direct the Examiner's attention to Applicants' Claim 2: "***transmitting, on a beat, 'K-F' bits of the 'K' bit group of data, using the 'K-F' nonfaulty conductors***". Olsen and Izuno do not transmit a portion of a "K" bit group... each transmits the entire "K" bit group, using either spare bits or a separate bus. Furthermore, Claim 2 states: "***storing the "F" bits in the "K" bit group that cannot be transmitted, on the beat, due to "F" faulty conductors in the signaling bus***;" Olsen stores **no** data, as admitted by the Examiner, while Izuno stores **all** bits until successful receipt of the entire "J" bit block. Claim 2 continues: "***transmitting the stored "F" bits on one or more additional beats, using one or more of the "K-F" nonfaulty signaling conductors***." Olsen uses no additional beats; Izuno uses a separate bus and does not use one or more of the "K-F" nonfaulty signaling conductors of the signaling bus having "K" signaling conductors where zero to "K-1" of the signaling conductors is faulty as recited in Claim 1 from which Claim 2 depends. Izuno furthermore does not send the stored "F" bits on one or more additional beats, since Izuno always involves a fixed number of beats to successfully transmit the block of data. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw his rejection of Claim 2.

The Examiner rejects, in the same paragraph of the Office Action, Claims 6-7. Claim 6 depends directly from Claim 2 and indirectly from Claim 1; Claim 7 depends directly from Claim 1. Applicants submit that Claims 1 and 2 are allowable as described above.

Applicants directly respond to the rejection of Claim 6 now. Claim 6 includes the steps of: "***storing, in the second electronic unit, 'K-F' bits per beat for 'J/(K-F)' beats; and storing remainder bits in an additional beat, if 'J/(K-F)' results in a remainder***." Olsen and Izuno, separately or combined have absolutely no teaching of this limitation. Olsen teaches of a receiving unit receiving "K" bits per beat, using a spare link if required, to specifically eliminate the possibility of less than a transmission of "K" bits per beat. Izuno

simply sends the data over a nonfaulty bus, using the full "K" bits per beat. Both references are utterly silent with regard to accumulating data from the transmitter at anything less than what they would receive on a nonfaulty bus. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw his rejection of Claim 6.

Claim 7 includes the steps of: "***selecting a 'K-F' bit group of bits from the 'J' bit block of data on the first electronic unit; transmitting the 'K-F' bit group of bits from the first electronic unit to the second electronic unit using the 'K-F' nonfaulty signaling conductors in the signaling bus, using a beat of the signaling bus***;" Clearly, this claim element alone distinguishes over Olsen and Izuno, alone or in combination. Both references **always select the same number of bits for transmission** and do **not** select a different number of bits to transmit using a number of faults detected. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw his rejection of Claim 7.

On page 4 of the Office Action, the Examiner discusses his rejection of Claims 8-11 under 35 U.S.C. 103(a). Claim 8 is an apparatus claim corresponding to method Claim 1. The Examiner applies Olsen and Izuno as with the rejection of Claim 1 and its dependents. Applicants refer to the explanation above as to how Olsen and Izuno can not properly be used to reject Claims 8-11, as they do not, separately to together, teach, suggest, or motivate the limitations found in Claims 8-11.

On page 6 of the Office Action, the Examiner rejects Claims 3 and 12 under 35 U.S.C. 103(a) as being unpatentable over Olsen (US 5,440, 538), Izuno et al. (US 5,717,852) further in view of Becker et al. (US 2004/0136319A1). These will be, respectively, be referred to as Olsen, Izuno, and Becker.

Applicants submit that Claim 3, being dependent from Claim 1 which Applicants submit is allowable, is also allowable, along with dependent Claims 4 and 5. A further discussion of why a rejection of why Claim 3 (and Claims 4, 5) are allowable over Olsen, Izuno, and Becker, is given below.

Applicants point out that Becker, as with Olsen and Izuno do not teach a signaling bus that does not have one or more spare signaling conductors. For example, Becker relies upon a spare signaling conductor (206, in Fig. 2) and transmission of a varying number of bits

depending on number of faulty signaling conductors is not taught in Becker, or, as explained above, in Olsen or in Izuno.

The Examiner relies on Becker for a "shift register unit (e.g., items 402-406, fig. 4) for storing data bits.

Applicants respectfully point out that shift register bits 402-406 are not connected in a manner wherein bits in the shift register can even be driven on a signaling bus. Rather, Becker's shift register is used by Becker's test control logic 434 to provide data that is compared against data received on Becker's chip from receivers 414, 416, and 418. No teaching is made, as required in Claim 3, of shifting "at least one bit of the 'F' bits into a first end of a shift register." "F" bits are bits that would have been transmitted in a beat, but were directed to faulty signaling conductors and therefore could not be transmitted on the same beat that data was transmitted over nonfaulty signaling conductors. Applicants respectfully submit that the fact that Becker "has a shift register" does not make obvious the use of a shift register as claimed in Claim 3 to store bits that would have been transmitted on a particular beat, but for a fault on a signaling conductor.

The Examiner specifically cites [0007] in Becker as to Becker's motive: "...to handle defects or failures in signal paths between different chips". Becker does in fact handle defects or failures in signal paths between different chips. Becker accomplishes this by using redundant signal paths as explained above. Applicants submit that Applicants' Claims 3-5 clearly distinguish over Becker alone or in combination with Olsen and Izuno.

On page 6 of the Office Action, the Examiner, arguing for rejection of Claim 12 states that Becker teaches a method for "*managing a set of signal paths between a driver chip (e.g. item 100, fig. 1) and a receiver chip (e.g. item 102, fig. 1) comprising a testing system included a shift register unit (e.g. items 402-406 for storing data bits.*"

Applicants first submit that Claim 12 depends indirectly from Claim 8, which Applicants believe is allowable, thereby making Claim 12 also allowable.

Applicants respectfully submit that "*managing a set of signal paths*" does not teach storing a number of bits, the number variable dependent upon number of faults on the signaling bus. Nor does it teach storing even fewer bits in the case of a remainder. These are claim limitations of Claim 12. Olsen and Becker also do not teach of storing a variable

number of bits dependent upon number of faults on the signaling bus. In fact, as described earlier, Olsen and Becker always receive the same number of bits, the same number of bits provided either by redundant signaling conductors or by a completely separate signaling bus. Applicants respectfully request that the Examiner reconsider and withdraw his rejection of Claim 12.

On page 7 of the Office Action, the Examiner rejects Claims 14-16 under 35 U.S.C. 103(a) as being unpatentable over Olsen and in further view of Becker et al.

Claims 14-16 depend from Claim 13, which Applicants submit is allowable, thereby also making Claims 14-16 allowable.

The Examiner states that "As per claim 14: Olsen teach(*sic*) a method as in claim 13 above but fails to teach the nonfaulty signaling conductors are identified during a power on sequence." Applicants agree that identification of faulty/nonfaulty signaling conductors being identified during a power on sequence is well known. In fact, "wire test", [0009] in Applicants' specification, is routinely done during power on sequence, and has been for many years. Nonetheless, Applicants submit that Claim 14 is allowable by virtue of dependence from Claim 13.

On page 7 of the Office Action, the Examiner states that "*Claim 15: Olsen and Becker teach a method as in claim 13 above, wherein the nonfaulty signaling conductors are identified by a wire test performed as a result of a parity error, and error correcting code error, or a cyclical redundancy check error (e.g. [0039] & [0044]); Becker et al.)*" Applicants agree that performing wire test in response to a signaling bus error is done routinely, but not in combination with the teachings of Claim 13, which Applicants submit is clearly distinguishable over the art cited and is allowable, therefore making Claim 15 also allowable.

On page 8 of the Office Action, the Examiner argues for rejection of Claim 16. Applicants note that the cited paragraph [0018] in Becker is silent with regard to Applicants' claim limitation of "switching a driver coupled to the faulty signaling conductor to a high impedance state." In fact, Becker, [0018] states, in its entirety, "*During a manufacturing test or during functional operation, if any signal path in bus 104 is detected or diagnosed to be defective, signaling is re-routed around the defective signal path by activating or switching*

into operation spare bit line 106." Applicants respectfully submit that teaching of switching a driver to a high impedance state upon identifying that the signaling conductor is faulty is not taught in Becker.

Applicants further submit that Claim 16 is allowable by virtue of its dependence from Claim 13.

IV. Conclusion

In view of the foregoing comments and amendments, Applicant respectfully requests that the application, with Claims 1-16 be passed to issue.

If the Examiner believes that a telephone interview with Applicants' agent would be helpful in speeding prosecution, Applicants' agent would encourage a telephone interview at the number below.

Respectfully submitted,

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